What is claimed is:

1. A data processor on a semiconductor substrate comprising:

a plurality of internal circuits including a nonvolatile memory and a central processing unit,

wherein the nonvolatile memory comprises a memory array including electrically erasable and writable nonvolatile memory cells, each of which includes a gate insulating film, a charge storage insulating film for storing information and over the gate insulating film, a memory gate electrode over the charge storage insulating film,

wherein the memory array includes a specific storage region capable of reading data stored in the memory cells therein in response to a reset instruction, and

wherein the data read from said specific storage region is repair information for replacing a normal storage region in a predetermined internal circuit with a redundant storage region in the predetermined internal circuit.

2. A data processor on a semiconductor substrate comprising:

a plurality of internal circuits including a nonvolatile memory and a central processing unit,

wherein the nonvolatile memory comprises a memory array including electrically erasable and writable nonvolatile memory cells, each of which includes a gate

insulating film, a charge storage insulating film for storing information and over the gate insulating film, a memory gate electrode over the charge storage insulating film,

wherein the memory array includes a specific storage region capable of reading data stored in the memory cells therein in response to a reset instruction, and

wherein the data read from the specific storage region is trimming information for adjusting characteristics of a predetermined internal circuit.

3. A data processor on a semiconductor substrate comprising:

a plurality of internal circuits including a nonvolatile memory and a central processing unit,

wherein the nonvolatile memory comprises a memory array including electrically erasable and writable nonvolatile memory cells, each of which includes a gate insulating film, a charge storage insulating film for storing information and over the gate insulating film, a memory gate electrode over the charge storage insulating film, and

wherein the data processor comprises an input terminal of an operation mode signal for selectively designating a first mode of allowing a predetermined internal circuit to control rewriting of information stored in said nonvolatile memory or a second mode of allowing an external device

connected to the data processor to control the rewriting.

4. The data processor according to claim 1,

wherein the nonvolatile memory cell comprises a first transistor part used for storing information and a second transistor part for selecting the first transistor part,

wherein the first transistor part is of an MONOS type including the charge storage insulating film and a memory gate electrode, and

wherein the second transistor part is of an MOS type.

5. The data processor according to claim 4,

wherein a channel region of the first transistor part and a channel region of the second transistor part are adjacent to each other, and

wherein a gate insulating withstand voltage of the second transistor part is lower than that of the first transistor part.

6. The data processor according to claim 4,

wherein a channel region of the first transistor part and a channel region of the second transistor part are adjacent to each other, and

wherein a gate insulating film of the second transistor part has the same thickness as that of a gate insulating film of an MOS type transistor as a component of the central processing unit.

7. The data processor according to claim 5,

wherein the first transistor part includes a source line electrode connected to a source line, the memory gate electrode connected to a memory gate control line, and the charge storage insulating film disposed directly below the memory gate electrode, and

wherein the second transistor part includes a bit line electrode connected to a bit line and a control gate electrode connected to a control gate control line.

8. The data processor according to claim 7, further comprising:

a switch MOS transistor capable of coupling the bit line to a global bit line,

wherein a gate oxide film of the switch MOS transistor is thinner than that of the first transistor part.

9. The data processor according to claim 8, comprising:

a first driver for driving the control gate control line;

a second driver for driving the memory gate control line;

a third driver for driving the switch MOS transistor to an on state; and

a fourth driver for driving the source line,

wherein the first and third drivers use a first voltage

as an operation power source, and the second and fourth drivers use a voltage higher than the first voltage as an operation power source.

10. The data processor according to claim 9, further comprising:

a control circuit, at the time of increasing a threshold voltage of said first transistor part, for setting the operation power source of the first driver as a first voltage, setting the operation power source of the fourth driver as a second voltage higher than the first voltage, setting the operation power source of the second driver as a third voltage higher than the second voltage, and enabling hot electrons to be injected from a bit line electrode side into a charge storage region.

11. The data processor according to claim 10, wherein at the time of decreasing the threshold voltage of the first transistor part, the control circuit sets the operation power source of the second driver as a fourth voltage higher than the third voltage, and discharges electrons from the charge storage region to the memory gate electrode.

12. The data processor according to claim 11, wherein the first transistor part whose threshold voltage is set to be low is of a depletion type, and the first transistor part whose threshold voltage is set to be high is of an enhancement

type.

13. A data processor on a semiconductor substrate comprising:

a plurality of internal circuits including a nonvolatile memory and a central processing unit, and

an input terminal of an operation mode signal for selectively designating a first mode of allowing a first internal circuit to control rewriting of information stored in the nonvolatile memory or a second operation mode of allowing an external device coupled to the data processor to control the rewriting,

wherein the nonvolatile memory comprises a memory array including electrically erasable and writable nonvolatile memory cells, each of which includes a gate insulating film, a charge storage insulating film for storing information and over the gate insulating film, a memory gate electrode over the charge storage insulating film,

wherein the memory array includes a specific storage region capable of reading data stored in the memory cells therein in response to a reset instruction, and

wherein the data read from said specific storage region includes:

repair information for replacing a normal storage region in a second internal circuit with a redundant storage region in the second internal circuit, and

trimming information for adjusting characteristics of a third internal circuit.